REMARKS

An Information Disclosure Statement is submitted herewith.

In the Office Action dated November 24, 2004, claims 1-17 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,745,064 (Ohya) in view of U.S. Patent No. 5,105,193 (Vogt).

Claim 1 of the patent application as filed relates to a two-dimensional matrix decoder for a digital-to-analog converter comprising an array of current cells. The current cells have a current source means or a current divider means and a switching means. The current cells are activatable in a pre-determined sequence.

The matrix decoder comprises:

- a selection means for outputting a first selection signal for selecting a cell;
- a cell state signalling means for outputting a cell state signal determining whether a cell comes before or after the selected cell in the predetermined sequence; and
- a matrix logic unit associated with each cell for generating a control signal suitable for controlling the switching means of that cell for switching current from the current source means or current divider means of that cell to at least one of a first node or a second node, the control signal being generated depending on the first selection signal and the cell state signal.

The cell state signal according to the present invention reports the status of a cell, *i.e.* reports whether a cell comes before or after a selected cell in the pre-determined sequence. According to some embodiments, this may be useful at the moment of switching from one digital value to another: depending on the digital value, a first selection signal is generated for selecting a particular cell. Each cell receives its cell state signal, and thus knows whether, in the pre-determined sequence, it comes before or after the selected cell. According to some embodiments, all cells from the first in the sequence up to the selected cell are in the ON state. Cells coming after the selected cell are switched OFF. In such embodiments, at the moment of switching from one digital value to another, each cell can determine from the first selection signal and the cell state signal to which node the current from its current source means or current divider means has to be switched.

U.S. Patent No. 5,745,064 discloses a two-dimensional matrix decoder (435e) for a digital-to-analog converter comprising an array (437e) of current cells (436). The current cells (436) in the array (437e) have a current source means (451) and a switching means (452, 453).

The matrix decoder comprises:

- a selection means (431a, 431b) for outputting a first selection signal (401, 402) for selecting a number of cells (436), and
- a matrix logic unit (450) associated with each cell (436) for generating a control signal suitable for controlling the switching means (452, 453) of that cell (436) for switching current from the current source means (451) of that cell (436) to at least one of a first node (433a) or a second node (434a).

U.S. Patent No. 5,745,064 does not disclose that the matrix decoder comprises a cell state signaling means outputting a cell state, *i.e.* a signal determining whether a cell comes before or after the selected cell in a pre-determined sequence. Neither does it disclose that the control signal for controlling the switching of the current sources in the cells would be generated depending on the first selection signal and the cell state signal. Rather the first selection signal by itself determines which current sources are to be connected to which nodes.

Contrary to the Examiner's opinion, neither does U.S. Patent No. 5,105,193 disclose such cell state signaling means.

U.S. Patent No. 5,105,193 discloses a DAC comprising column decoding means (1) and row decoding means (2), as well as a matrix (4) of cells, each cell comprising a current source (8), the current sources of the plurality of cells being arranged to supply a current of a pre-determined magnitude to a common output path. Each cell furthermore comprises a local decode circuit (6) responsive to one column address bit and its inverse and two row address bits and their inverses to set the condition of a pair of cross-coupled p-channel devices (9, 10). Each cell of the DAC described furthermore comprises a switch drive circuit (7) comprising a pair of series n-channel devices which, during transitions between one coded input signal and the next, are switched to a non-conducting condition by means of a control signal applied in common to all cells of the matrix by way of a path. A half-latch circuit maintains the current sources in their existing state. Once the decoding circuits have settled, thus have taken the new values, the pair of series n-channel devices in all cells are switched into conduction substantially simultaneously

by way of the path, whereby the half-latches and the current sources in all cells are switched substantially simultaneously to the condition required by the new digitally coded input signal.

This means that in U.S. Patent No. 5,105,193, no cell state signaling means are provided, which cell state signaling means output a cell state signal determining whether a cell comes before or after the selected cell in the predetermined sequence.

Contrary to the Examiner's opinion, the state of the cells is not determined in U.S. Patent No. 5,105,193. No cell state signal is delivered which can be used for generating a control signal for controlling the switching means of a cell.

Therefore, even if the matrix decoder of U.S. Patent No. 5,745,064 could be combined with a device according to the teaching of U.S. Patent No. 5,105,193 (which is contested), the hypothetical combination of these references would not teach or suggest all elements of the claim.

In such an alleged combination a cell state signaling means would not output a cell state signal determining whether a cell comes before or after the selected cell in the predetermined sequence. Accordingly, no use is described of this signal inside a cell, together with a first selection signal selecting a cell, for generating a control signal for controlling the switching means of that cell. The selection signal generated in accordance with U.S. Patent No. 5,745,064 is used directly for controlling the switching means of the cells, because this selection signal directly determines the number and the location of current sources to be switched ON.

Therefore, in view of the above, a *prima facie* case of obviousness has not been established with respect to claim 1. *See* M.P.E.P. § 2143 (8th ed., Rev. 2), at 2100-129.

Claims 2 to 9 are also allowable in view of their dependency on claim 1.

An analogous reasoning holds for claim 11. None of the prior art documents determines whether a cell comes before or after a selected cell in a pre-determined sequence. Neither does any of the prior art documents hint in that direction. Therefore, a *prima facie* case of obviousness has also not been established with respect to claim 11.

Claims 12 to 17 are also allowable in view of their dependency on claim 11.

Claim 10 relates to a DAC comprising the matrix decoder in accordance with claim 1. As this matrix decoder, as explained above, is considered to contain novel and inventive features, claim 10 is also allowable.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 20-1504 (BGC.0005US).

Respectfully submitted,

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